This listing of claims replaces all prior versions and listings of claims in the application.

In the Claims:

1. (currently amended) An insulated gate field effect transistor, comprising:

a source and, a drain predominantly having a first dopant type selected from n and p type dopants, and a transistor body including a channel predominantly having a second dopant type selected from the n and p type dopants, the second dopant type opposite the first dopant type, the source, drain and transistor body being disposed ~~formed~~ in a layer of a single-crystal semiconductor, overlying ~~said layer disposed over~~ and insulated from a bulk semiconductor layer of a substrate by a buried insulator layer;

a gate conductor disposed in an annular pattern overlying said channel, such that said gate conductor surrounds one of said source and said drain disposed to the inside of said annular pattern, the other of said source and said drain being disposed to the outside of said annular pattern, said gate conductor further including a second pattern connected to said annular pattern; and

a conductive body contact including a body contact region in ~~to~~ said single-crystal semiconductor layer in the vicinity of said second pattern, said body contact region having predominantly said second dopant type, said body contact region providing a low resistance path for flow of charge carriers to and from said transistor body.

2. (currently amended) The insulated gate field effect transistor of claim 1, wherein said source, drain and ~~channel region~~ transistor body are disposed in an active

area of said single-crystal semiconductor layer bounded by one or more isolation structures.

3. (original) The insulated gate field effect transistor of claim 1, wherein said second pattern extends linearly between said annular pattern and an edge of said active area.

4. (original) The insulated gate field effect transistor of claim 1, wherein said annular pattern includes a pair of parallel portions oriented in a first direction substantially parallel to an edge of said active area and further includes angled portions oriented at an angle to said first direction.

5. (original) The insulated gate field effect transistor of claim 4, wherein at least some of said angled portions are oriented at angles between about 30 degrees and 60 degrees with respect to said first direction.

6. (original) The insulated gate field effect transistor of claim 4, wherein at least some of said angled portions are oriented at angles of about 45 degrees.

7. (currently amended) The insulated gate field effect transistor of claim 1, wherein said transistor is an n-type FET, the source is disposed to the outside of the

annular pattern, and ~~the~~ said body contact region is disposed ~~on a region of said layer~~ adjacent to said source.

8. (currently amended) The insulated gate field effect transistor of claim ~~1~~ 2, wherein said gate conductor further includes a third pattern connected to said annular pattern, said second and third patterns extending from first and second locations of said annular pattern in substantially opposite directions.

9. (original) The insulated gate field effect transistor of claim 8, wherein said second and said third patterns extend linearly between said annular pattern and edges of said active area.

10. (currently amended) An insulated gate field effect transistor, comprising:

a source and~~,~~ a drain predominantly having a first dopant type selected from n and p type dopants, and a transistor body including a channel predominantly having a second dopant type selected from the n and p type dopants, the second dopant type opposite the first dopant type, the source, drain and transistor body being disposed ~~formed~~ in a layer of a single-crystal semiconductor~~,~~ overlying ~~said layer disposed over~~ and insulated from a bulk semiconductor layer of a substrate by a buried insulator layer;

a gate conductor including a first multiple finger pattern overlying said channel and a second multiple finger pattern overlying said channel, and a connecting pattern conductively connecting said first and second multiple finger patterns; and

an electrically conductive body contact including a body contact region in ~~to~~ said single-crystal semiconductor layer disposed in the vicinity of said connecting pattern, said body contact region having predominantly said second dopant type, said body contact region providing a low resistance path for flow of charge carriers to and from said transistor body.

11. (original) The insulated gate field effect transistor of claim 10, wherein said first and said second multiple finger patterns each have two fingers, wherein one of said source and said drain is disposed between said two fingers, and the other of said source and said drain is disposed to the outside of said two fingers.

12. (original) The insulated gate field effect transistor of claim 10 wherein said gate conductor includes four fingers.

13. (currently amended) The insulated gate field effect transistor of claim 10 wherein said gate conductor includes a multiple ~~n~~ N of two fingers, wherein ~~n~~ N is greater than two.

14. (currently amended) The insulated gate field effect transistor of claim 10, wherein said source, drain and ~~channel region~~ transistor body are disposed in an active area of said layer bounded by one or more isolation structures.

15. (currently amended) The insulated gate field effect transistor of claim 10, wherein said transistor is an n-type FET, and said source is disposed to the outside of the annular pattern, and ~~the~~ said body contact region is disposed ~~on a region of said layer~~ adjacent to said source.

16. (currently amended) A method of making an insulated gate field effect transistor, comprising:

providing a substrate having a single-crystal semiconductor layer separated from a bulk semiconductor portion by a buried insulator layer;

forming a source and~~,~~ a drain predominantly having a first dopant type selected from n and p type dopants, and a transistor body including a channel predominantly having a second dopant type selected from the n and p type dopants, the second dopant type opposite the first dopant type, the source, drain and transistor body being disposed ~~formed~~ in said single-crystal semiconductor layer;

forming a gate conductor disposed in an annular pattern overlying said channel, such that said gate conductor surrounds one of said source and said drain disposed to the inside of said annular pattern, the other of said source and said drain being disposed to the outside of said annular pattern, said gate conductor further including a second pattern connected to said annular pattern; and

forming an electrically conductive body contact including a body contact region in ~~to~~ said single-crystal semiconductor layer in the vicinity of said second pattern, said body contact region having predominantly said second dopant type, said body contact

region providing a low resistance path for flow of charge carriers to and from said transistor body.

17. (currently amended) The method of claim 16 wherein said gate conductor is patterned to form said annular pattern and said second pattern prior to depositing at least one material selected from the group consisting of heavily doped polysilicon, metals and metal compounds to form said electrically conductive body contact.

18. (original) The method of claim 17 wherein said material is deposited prior to implanting ions to form said source, and said drain, said channel remaining as an area disposed under at least portions of said gate conductor between said source and said drain.

19. (currently amended) The method of claim 15, further comprising:

patterning an active area in said single-crystal semiconductor layer;

providing trench isolations to isolate said active area,

wherein said source, said drain, and said ~~channel~~ transistor body are formed in said active area.

20. (original) The method of claim 15, wherein said second pattern extends linearly between said annular pattern and an edge of said active area.